REMARKS

Claims 1-18 are presently pending and stand rejected. Claims 19-21 are cancelled without prejudice.

Claims 1-6, 11-12, and 13-18 were rejected under 35 U.S.C. § 102(b) as being anticipated by Kono.

Claim 1 recites, among other limitations, "a display manager for determining when to overwrite an existing image in the image buffers, and providing a signal to the decoder indicating when to overwrite the existing image in the frame buffer".

Examiner has indicated that Kono teaches "a display manager (55) for determining when to overwrite an existing image in the image buffers and providing a signal to the decoder indicating when to overwrite the existing image in the frame buffer (pg.6, [0075] and [0080]-[0081])". Office Action at 2.

Kono [0075], Lines 8-15 teaches that

> Further, the display control section 55 issues a display starting instruction to the frame memory 53. Based on this display starting instruction 68, a desired picture is transferred to a display unit not shown in Fig. 6 from the frame memory 53, and the picture is displayed in the display unit. After the completion of the display, the display control section 55 issues a display completion notice 74 to the status register 57.

Assignee respectfully submits that the claimed "overwrite an existing image in the image buffers" does not read on "a desired picture is transferred to a display unit". Mere transfer of an image from Kono, frame buffer 53

to a display unit, does not result in overwriting the picture in the frame buffer 53.

Moreover, Kono would be inoperable if an image from Kono, frame buffer 53 were immediately overwritten upon transfer to the display unit. Kono [0006] notes that "The B picture is coded by using past and future I picture or past and future P pictures as reference pictures. Therefore, the information of past and future I pictures or P pictures are necessary for decoding the B pictures." Thus, immediately overwriting a picture upon transfer to the display unit would overwrite the information of past I and P pictures that "are necessary for decoding the B pictures."

Additionally, the foregoing does not teach or fairly suggest that the display manager is "providing a signal to the decoder indicating when to overwrite the existing image in the frame buffer". Note that neither the "display starting instruction" or the "display completion notice" are "a signal to the decoder".

Kono [0080], Lines 5-9 merely recite:

> Parameters of each layer that have been generated as a result of the decoding are overwritten into the parameters stored in the MB buffer 58 (step S6). Then the parameters are transferred from the MB buffer to the parameter bank, and are written into this parameter bank.

Assignee respectfully submits that "overwrite an existing image" does not read on "Parameters of each layer that have been generated as a result of the decoding are overwritten". Moreover, even if it did, there is no

teaching that the foregoing is because of the display manager "providing a signal to the decoder indicating when to overwrite the existing image in the frame buffer". In Figure 6, the "Display Control Section 55" has only two outputs, the "Display Starting Instruction" and the "Display Completion Notice". As noted above, the "display starting instruction" and the "display completion notice" are not provided to the "image decoding section 52".

Accordingly, for these reasons alone, Assignee respectfully traverses the rejection to claim 1 and 13 and to dependent claims 2-12, and to dependent claims 14-18 and request that Examiner withdraw the rejection.

Claim 7 further recites, "wherein the second processor is off-chip from the integrated circuit". Examiner has indicated that "Kono et al fails to teach wherein the second processor is off-chip from the integrated circuit. However, Jiang et al in the same field of endeavor teaches wherein the second processor is off-chip from the integrated circuit as recited in claim 7 (col. 9, lines 44-47)". Office Action at 6.

Assignee respectfully traverses and notes that Jiang, Col. 9, Lines 44-47 merely teaches, "The display controller 540 retrieves the video data that is to be converted using the 3:2 pulldown technique from the DRAM 190 via the memory interface 520." It is noted that there is no teaching that the "display controller 540" is "off-chip from the integrated circuit". Moreover, Assignee calls Examiner's attention to Figure 5, where the "display controller 540"

is a part of the "video stream decoder 180" and clearly not shown "off-chip from the integrated circuit".

Conclusion

For the foregoing reasons, Assignee respectfully submits all of the pending claims are in a condition for allowance, thereby placing the application in a condition for allowance. It is believed that there is no fee associated with any of the actions requested herein. To the extent that there is any fee associated with any actions requested herein, the Commissioner is requested to charge such fee to deposit account 13-0017.

RESPECTFULLY SUBMITTED

October 26, 2007

Mirut Dalal - Reg. No. 44,052
ATTORNEY FOR ASSIGNEE

McAndrews, Held & Malloy, Ltd.
500 West Madison - Suite 3400
Chicago, IL 60661

Phone (312) 775-8000
FAX (312) 775-8100